REMARKS

In view of the above amendments and following remarks, reconsideration and further examination are requested.

Fig 1G has been amended to correctly identify the conductive particle bodies 10a-1 and the insulation layer 10a-2, and Figs 15, 16A and 16B have been labeled as "Prior Art"

The specification has been reviewed and revised to make editorial changes thereto and generally improve the form thereof. No new matter has been added by the revisions to the specification and abstract.

By the current Amendment claims 1-71 have been cancelled and claims 72-142 have been added. New claims 72-135 have been drafted taking into account the objection noted by the Examiner in section 2 on page 2 of the Office Action, and also taking into account the 35 U.S.C. § 112, second paragraph, rejection of claims 30 and 37-40. New claims 72-142 are believed to be free of the basis for this objection and rejection, and are otherwise believed to be in compliance with 35 U.S.C. § 112, second paragraph.

Claims 72-142 are believed to be allowable over the references relied upon by the Examiner to reject claims 25-27, 29, 30, 33, 36-40, 64 and 69 for the following reasons.

Claim 72 recites a method for mounting an electronic component that comprises *inter alia*

> while an insulating resin layer is interposed between said electronic component and a circuit board, mounting said electronic component onto said circuit board... wherein said insulating resin layer includes a mixture of an insulating resin, an inorganic filler and conductive particles.

Claim 109 recites an apparatus for mounting an electronic component that corresponds to method claim 72, and also recites that the insulating resin layer includes a mixture of an insulating resin, an inorganic filler and conductive particles.

Claims 72 and 109 are allowable over the references relied upon by the Examiner, either taken alone or in combination, because none of these references fairly teach or suggest the method of claim 72 or the apparatus of claim 109, wherein an insulating resin layer that includes a mixture of an insulating resin, an inorganic filler and conductive particles is interposed between an electronic

component and a circuit board while the electronic component is bonded to the circuit board via a bump on the electronic component.

In this regard, Nishida discloses a method and an apparatus for electrically connecting an electronic component 1 to a circuit board 4 via a bump 3 with an anisotropic conductive film 10 or a thermosetting resin sheet 6 interposed between the electronic component and the circuit board. The conductive film 10 may include conductive particles, e.g. nickel powder plated with gold (column 15, lines 39-45) and the resin sheet 6 may include an inorganic filler (column 13, lines 33-37). However, neither claim 72 nor claim 109 is anticipated by Nishida.

Specifically, with regard to the thermosetting resin sheet 6, while this sheet is disclosed to possibly include an inorganic filler, nowhere in Nishida is it disclosed that conductive particles are **mixed** with the material forming the sheet, such that the sheet is not "a mixture of an insulating resin, an inorganic filler and conductive particles", as recited in each of claims 72 and 109. While Figures 11A through 12H of Nishida show a thermosetting resin sheet in combination with conductive particles, these conductive particles are inserted into openings 15 provided through the resin sheet, such that the resin sheet is not a "mixture of an insulating resin, an inorganic filler and conductive particles" as required by each of claims 72 and 109.

And, with regard to the anisotropic conductive film 10 of Nishida, nowhere is this film disclosed to include an inorganic filler in addition to conductive particles 10a. Accordingly, the anisotropic conductive film 10, is also not a mixture of an insulating resin, an inorganic filler and conductive particles.

Accordingly, in view of the above, it is respectfully submitted that claims 72 and 109 are not anticipated by Nishida.

It is appreciated that Yamaguchi discloses an anisotropic electrically conductive adhesive film that includes an insulating adhesive, electrically conductive particles dispersed in the electrically insulating adhesive, and glass particles dispersed in the insulating adhesive. However, contrary to the position taken by the Examiner, it is respectfully submitted that there would have been no motivation or suggestion for one having ordinary skill in the art to have used the anisotropic film of Yamaguchi in the method of Nishida.

In this regard, the anisotropic adhesive film of Yamaguchi is used by itself to join an electronic component to a substrate, whereas in Nishida the anisotropic film 10 or thermosetting resin sheet 6 is used in combination with bumps 3 to join electronic component 1 to circuit board 4. Accordingly, because of the different manners by which the anisotropic films of Yamaguchi and Nishida are used with regard to joining an electronic component to a substrate, one having ordinary skill in the art would not have been motivated to substitute the anisotropic film of Yamaguchi for that of Nishida.

Additionally, even if one having ordinary skill in the art would have found it obvious to make such a substitution, then it is respectfully submitted that when making such a substitution the gold bumps 3 of Nishida would be eliminated as no longer being necessary, since as expressed previously the anisotropic film of Yamaguchi is by itself sufficient to electrically interconnect an electronic component to a substrate, whereby a combination of Nishida and Yamaguchi would not result in the invention as recited in claims 72 and 109.

In view of the above, it is respectfully submitted that claims 72 and 109 are also not obvious over a combination of Nishida and Yamaguchi.

The remaining references relied upon by the Examiner do not resolve the above deficiencies of Nishida and Yamaguchi, such that claims 72 and 109 are also allowable over any possible combination of the references relied upon by the Examiner. Thus, claims 72-142 are allowable over the references relied upon by the Examiner, either taken alone or in combination.

Additionally, certain of the dependent claims are believed to be patentable in their own right, as follows.

Claim 106 recites that the conductive particles are each surrounded by an insulation layer. This is shown in Figure 1G for example, where the conductive particle body 10a-1 is surrounded by insulation layer 10a-2. In Nishida, the conductive particles are not disclosed to be surrounded by any insulation layer. Similarly, in Yamaguchi, the electrically conductive particles are also not disclosed to be surrounded by any insulation layer. Thus, claim 106 is patentable in its own right.

Claim 81 recites that before mounting the electronic component onto the circuit board, a load of not greater than 20 gf is applied to the bump such that a tip of the bump is shaped but not collapsed. Nishida is silent with regard to applying any such load to bump 3, and accordingly, claim 81 is patentable in its own right.

Claim 107 recites that the inorganic filler comprises a first type of inorganic filler and a second type of inorganic filler. As recognized by the Examiner, Nishida does not disclose or suggest first and second types of filler, and thus relied upon Yamaguchi for teaching first and second types of inorganic filler. While the Examiner has equated the electrically conductive particles and the glass particles of Yamaguchi as first and second types of filler, claim 107 requires conductive particles, in addition to the first and second types of filler. Thus, claim 107 requires three distinct types of particles. Accordingly, because Yamaguchi only discloses two distinct types of particles, Yamaguchi cannot remedy the deficiency of Nishida as noted by the Examiner. Accordingly, claim 107 is patentable in its own right. For an analogous reason, claim 104 is also patentable in its own right.

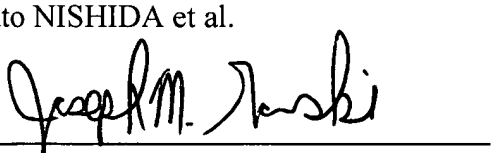
Claims 98 and 122 recite that bonding of the electronic component to the circuit board is to be performed by applying first and second pressures to the electronic component at different times, with the second pressure being less than the first pressure. Such a feature allows for stress to be alleviated in the circuit board and electronic component, and is not taught or suggested by any of the references relied upon by the Examiner. Accordingly, claims 98 and 122 are each patentable in its own right.

In view of the above amendments and remarks, it is respectfully submitted that the present application is in condition for allowance and an early Notice of Allowance is earnestly solicited.

If after reviewing this Amendment, the Examiner believes that any issues remain which must be resolved before the application can be passed to issue, the Examiner is invited to contact the Applicants' undersigned representative by telephone to resolve such issues.

Respectfully submitted,

Kazuto NISHIDA et al.

By: 

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